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09/961,055	09/24/2001	Masaaki Hiroki	740756-2367	6718

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EXAMINER	
PARKER, KENNETH	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/961,055	Applicant(s) HIROKI ET AL.
	Examiner Kenneth A. Parker	Art Unit 2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 June 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2,4,6-9,19,21 and 24-58 is/are pending in the application.

4a) Of the above claim(s) 19,21,24-36 and 48-58 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2,4,6-9 and 37-47 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/10/05, 3/14/05, 8/15/05, 6/26/05

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2,4,6, 7-9 and 37-42 and 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujikawa et al 5051570 in view of Woods 4007294 or Zhang EP0459763 A1 .

Tsujikawa discloses a liquid crystal device meeting all the claim limitations (see claim by claim discussion below) other than the fluorine in the gate insulator. Zhang teaches using fluoring (page 7, lines 15-35) for the benefit of terminating dangling bonds (see

abstract). Woods et al teaches treating the silicon dioxide with flourine to prevent problems do to ions (abstract). Therefore one of ordinary skill would have found reason, motivation and suggestion to employ fluorine for the benefits mentioned above. Regarding claim 2, the reference shows. An electro-optical display device comprising:

a first substrate having an insulating surface 128;

at least one thin film transistor 104 formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said gate insulating film (as shown with 113,115 and 135);

a leveling film comprising an organic resin formed over said at least one thin film transistor (123),

a pixel electrode 124 formed over said leveling film and electrically connected to one of said source and drain regions of the thin film transistor,

wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above).

The reference shows regarding claim 4 an electro-optical display device comprising

a first substrate having an insulating surface (128);

at least one thin film transistor 104 formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film adjacent to said channel region,

and a gate electrode adjacent to said gate insulating film (see above);

an interlayer insulating film formed over said thin film transistor, (122),

an electrode 118 formed on said interlayer insulating film and electrically connected to one of said source and drain regions,

a leveling film comprising an organic resin formed over said at least one thin film transistor (123),

a pixel electrode 124 formed over said leveling film and electrically connected to said one of said source and drain regions of the thin film transistor through said electrode, wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above).

The reference shows regarding claim 6 an electro-optical display device comprising:

a first substrate having an insulating surface 128;

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film over said channel region, and a gate electrode over said gate insulating film (see above),

an interlayer insulating film formed over said thin film transistor (see above);

an electrode formed on said interlayer insulating film and electrically connected to one of said source and drain regions,

a leveling film comprising an organic resin formed over said at least one

thin film transistor, (123)

a pixel electrode formed over said leveling film and electrically connected to said one of the source and drain regions of the thin film transistor through said electrode (see above),

wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above).

The reference shows regarding claim 7 an electro-optical display device comprising:

a first substrate having an insulating surface 128;

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending there between, a gate insulating film over said channel region, and a gate electrode over said gate insulating film (see above);

a leveling film comprising an organic resin formed over said at least one thin film transistor (see above),

a pixel electrode 124 formed over said leveling film and electrically connected to one of said source and drain regions of the thin film transistor (see above),

wherein said gate insulation film contains fluorine (met as modified by Woods or Zhang above).

The reference shows regarding claim 8 an electro-optical display device comprising:

a first substrate having an insulating surface (see above);

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said gate insulating film (see above);

an interlaver insulating film formed over said thin film transistor (see above)

an electrode (118) formed on said interlayer insulating film and electrically connected to one of said source and drain regions through a first contact hole of said interlayer insulating film,

a leveling film comprising an organic resin 123 formed over said at least one thin film transistor and said electrode,

a pixel electrode 124 formed over said Leveling film and electrically connected to said one of said source and drain regions of the thin film transistor through said electrode (see above)

wherein said pixel electrode contacts said electrode through a second contact hole of said Leveling film (see the connection of the transistor);

wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above).

and said second contact hole

does not overlap said first contact hole (note that the hole through 123 is not aligned with the hole throguh 122).

The reference shows regarding claim 9 an electro-optical display device comprising:

a first substrate having an insulating surface(see above);

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film over said channel region, and a gate electrode ' over said gate insulating film (see above);

an interlayer insulation film formed over said thin film transistor (see above).

an electrode (118) formed on said interlayer insulation film and electrically connected to one of said source and drain regions through a first contact hole of said interlayer insulating film (see above),

a leveling film comprising an organic resin formed 123 over said at least one thin film transistor and said electrode,

a pixel electrode 124 formed over said leveling film and electrically connected to said one of said source and drain regions of the thin film transistor through said electrode wherein said pixel electrode contacts said electrode through a second contact hole of said leveling film;

wherein said gate insulation film 121 contains fluorine (met as modified by Woods or Zhang above), and said second contact hole does not overlap said first contact hole (see above).

The reference shows regarding claim 37 a camera (as a preamble limitation, camera is met by a device which can be used in a camera, which the primary reference can and

further even has photosensors) having an active matrix type display device, said active matrix type display device comprising:

a first substrate having an insulating surface 128;

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending there between, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said gate insulating film (TFT 104 as shown with 113,115 and 135);

a leveling film comprising an organic resin formed over said at least one thin film transistor 123,

a pixel electrode 124 formed over said leveling film and electrically connected to one of said source and drain regions of the thin film transistor,

wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above).

The reference shows regarding claim 38 a camera (as a preamble limitation, camera is met by a device which can be used in a camera, which the primary reference can and further even has photosensors) having an active matrix type display device, said active matrix type display device comprising:

a first substrate having an insulating surface 128;

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel

region extending therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said gate insulating film (TFT 104 as shown with 113,115 and 135);

an interlayer insulating film 123 formed over said thin film transistor,

an electrode 118 formed on said interlayer insulating film and electrically connected to one of said source and drain regions,

a leveling film comprising an organic resin formed over said at least one thin film transistor

a pixel electrode formed over said leveling film and electrically connected to said one of said source and drain regions of the thin film transistor through said electrode, wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above).

The reference shows regarding claim 39 a camera (as a preamble limitation, camera is met by a device which can be used in a camera, which the primary reference can and further even has photosensors) having an active matrix type display device, said active matrix type display device comprising:

a first substrate having an insulating surface 128;

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film over said channel region, and a gate electrode over said gate insulating film (TFT 104 as shown with 113,115 and 135);

an interlayer insulating film formed over said thin film transistor 123,

an electrode formed on said interlayer insulating film and electrically connected to one of said source and drain regions,

a leveling film comprising an organic resin formed over said at least one thin film transistor,

a pixel electrode 124 formed over said leveling film and electrically connected to said one of the source and drain regions of the thin film transistor through said electrode,

wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above).

The reference shows regarding claim 40 a camera (as a preamble limitation, camera is met by a device which can be used in a camera, which the primary reference can and further even has photosensors) having an matrix type display device comprising:

active matrix type display device, said active

a first substrate having an insulating surface 128;

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film over said channel region, and a gate electrode over said gate insulating film (TFT 104 as shown with 113,115 and 135);

a leveling film comprising an organic resin formed over said at least one thin film transistor 123,

a pixel electrode 124 formed over said leveling film and electrically connected to one

of said source and drain regions of the thin film transistor,

wherein said gate insulating film contains fluorine ((met as modified by Woods or Zhang above).

The reference shows regarding claim 41 a camera (as a preamble limitation, camera is met by a device which can be used in a camera, which the primary reference can and further even has photosensors) having matrix type display device comprising

an active matrix type display device, said active

a first substrate having an insulating surface 128;

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said gate insulating film (TFT 104 as shown with 113,115 and 135);

an interlayer insulating film formed over said thin film transistor',

an electrode 118 formed on said interlayer' insulating film and electrically connected to one of said source and drain regions through a first contact hole of said interlayer insulating film;

a leveling film comprising an organic resin formed over said at least one thin film transistor and said electrode 123 ,

a pixel electrode 124 formed over said leveling film and electrically connected to said one of said source and drain regions of the thin film transistor through said electrode

wherein said pixel electrode contacts said electrode through a second contact hole of said leveling film;

wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above), and said second contact hole does not overlap said first contact hole (see discussion above).

The reference shows regarding claim 42 a camera (as a preamble limitation, camera is met by a device which can be used in a camera, which the primary reference can and further even has photosensors) having an matrix type display device comprising:

active matrix type display device, said active a first substrate having an insulating surface 128;

at least one thin film transistor formed over said first substrate, said thin film transistor comprising a channel region, source and drain regions with said channel region extending therebetween, a gate insulating film over said channel region, and a gate electrode over said gate insulating film (TFT 104 as shown with 113,115 and 135);

an interlayer insulating film formed over said thin film transistor,

an electrode formed on 118 said interlayer insulating film and electrically connected to one of said source' and drain regions through a first contact hole of said interlayer insulating film,

a leveling film comprising an organic resin formed over said at least one thin film transistor and said electrode 123,

a pixel electrode 124 formed over said leveling film and electrically connected to said

one of said source and drain regions of the thin film transistor through said electrode wherein said pixel electrode contacts said electrode through a second contact hole of said leveling film,

wherein said gate insulating film contains fluorine (met as modified by Woods or Zhang above), and said second contact hole does not overlap said first contact hole.

The reference shows regarding claim 44 the camera according to any one of claims 37-42 further comprising a liquid crystal and a second substrate wherein said liquid crystal is disposed between said first substrate and said second substrate (shown by the reference).

The reference shows regarding claim 45 the camera according to any one of claims 37-42 wherein said leveling film comprises polyimide (column 15, lines 20-25 and elsewhere).

The reference shows regarding claim 46 the camera according to any one of claims 37-42 wherein said channel region comprises crystalline silicon (column 13, lines 15-25).

The reference shows regarding claim 47 the camera according to any one of claims 37-42 wherein said gate insulating film comprises silicon oxide (column 9, lines 15-16).

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujikawa et al 5051570 in view of Shannon 5268679.

Lacking from Tsujikawa et al is the device having a pixel electrode which is transparent. Shannon dislcoses a multilayer optical device, where each layer is transparent (column1 lines27-52), and therefore must have transparent pixel electrodes. Shannon discloses that enables stacking of the device (columns 1-2), which enables implementation of thing like neural network (discussed in the background of the invention). Therefore one of ordinary skill would have found reason, motivation and suggestion to modify the device of Tsujikawa to employ a transparent pixel electrode such as Shannon for the reasons stated above.

Election/Restrictions

Applicant's election without traverse of group 3 in the reply filed on 6/28/05 is acknowledged.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier

communications from the examiner should be directed to Kenneth A. Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth A Parker
Primary Examiner
Art Unit 2871